

**Features**

- 128Kx8-bit Organization
- Address Access Time: 90 ns
- Single 5V  $\pm$  10% Power Supply
- Sector Erase Mode Operation
- 512 bytes per Sector, 256 Sectors
  - Sector-Erase Cycle Time: 10ms (Max)
  - Byte-Program Cycle Time: 30 $\mu$ s (Max)
- Minimum 1,000 Erase-Program Cycles
- Low power dissipation
  - Active Read Current: 20mA (Typ)
  - Active Program Current: 30mA (Typ)
  - Standby Current: 100 $\mu$ A (Max)
- Low V<sub>CC</sub> Program Inhibit Below 3.2V
- Self-timed program/erase operations
- CMOS and TTL Interface
- Packages:
  - 32-pin Plastic DIP
  - 32-pin PLCC

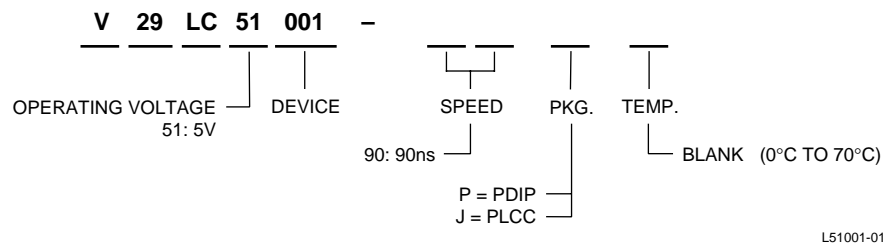
**Description**

The V29LC51001 is a high speed 131,072 x 8 bit CMOS flash memory. Programming or erasing the device is done with a single 5 Volt power supply. The device has separate chip enable  $\overline{CE}$ , program enable  $\overline{WE}$ , and output enable  $\overline{OE}$  controls to eliminate bus contention.

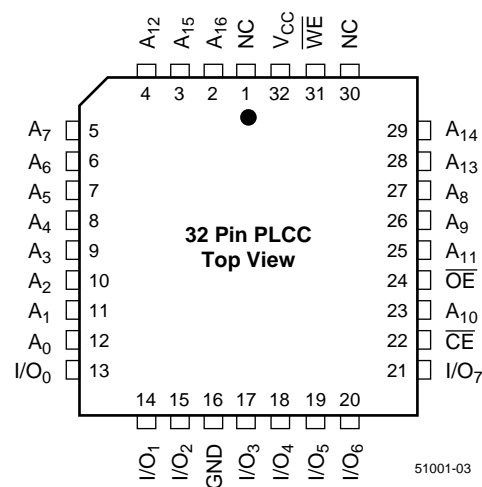
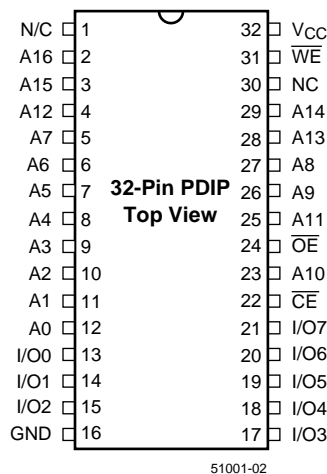
The V29LC51001 features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. The device also supports full chip erase.

**Device Usage Chart**

Operating Temperature Range	Package Outline		Access Time (ns)	Temperature Mark
	P	J	90	
0°C to 70°C	•	•	•	Blank



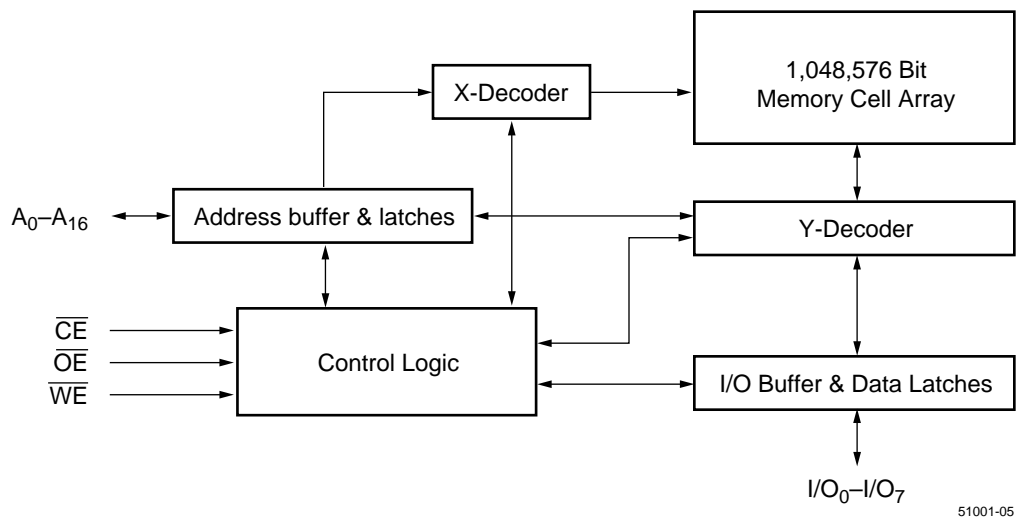
# Pin Configurations



# Pin Names

A <sub>0</sub> -A <sub>16</sub>	Address Inputs
I/O <sub>0</sub> -I/O <sub>7</sub>	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Program Enable
V <sub>CC</sub>	5V ± 10% Power Supply
GND	Ground
NC	No Connect

Functional Block Diagram



Capacitance (1,2)

Symbol	Parameter	Test mSetup	Typ.	Max.	Units
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	6	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	8	12	pF
C <sub>IN2</sub>	Control Pin Capacitance	V <sub>IN</sub> = 0	8	10	pF

NOTE:

- 1. Capacitance is sampled and not 100% tested.
- 2. T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5V ± 10%, f = 1 MHz.

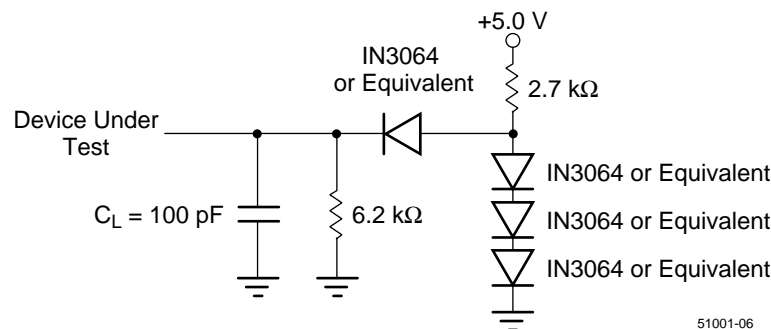
Latch Up Characteristics(1)

Parameter	Min.	Max.	Unit
Input Voltage with Respect to GND on A <sub>9</sub> , $\overline{OE}$	-1	+13	V
Input Voltage with Respect to GND on I/O, address or control pins	-1	V <sub>CC</sub> + 1	V
V <sub>CC</sub> Current	-100	+100	mA

NOTE:

- 1. Includes all pins except V<sub>CC</sub>. Test conditions: V<sub>CC</sub> = 5V, one pin at a time.

AC Test Load



**Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Parameter	Commercial	Unit
$V_{IN}$	Input Voltage (input or I/O pins)	-2 to +7	V
$V_{IN}$	Input Voltage ( $A_9$ pin, $\overline{OE}$ )	-2 to +13	V
$V_{CC}$	Power Supply Voltage	-0.5 to +5.5	V
$T_{STG}$	Storage Temperature (Plastic)	-65 to +125	°C
$T_{OPR}$	Operating Temperature	0 to +70	°C
$I_{OUT}$	Short Circuit Current <sup>(2)</sup>	200 (Max.)	mA

**NOTE:**

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. No more than one output maybe shorted at a time and not exceeding one second long.

**DC Electrical Characteristics**

(over the commercial operating range)

Parameter Name	Parameter	Test Conditions	Min.	Max.	Unit
$V_{IL}$	Input LOW Voltage	$V_{CC} = V_{CC} \text{ Min.}$	—	0.8	V
$V_{IH}$	Input HIGH Voltage	$V_{CC} = V_{CC} \text{ Max.}$	2	—	V
$I_{IL}$	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}, V_{CC} = V_{CC} \text{ Max.}$	—	$\pm 1$	$\mu\text{A}$
$I_{OL}$	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}, V_{CC} = V_{CC} \text{ Max.}$	—	$\pm 10$	$\mu\text{A}$
$V_{OL}$	Output LOW Voltage	$V_{CC} = V_{CC} \text{ Min.}, I_{OL} = 2.1\text{mA}$	—	0.4	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = V_{CC} \text{ Min.}, I_{OH} = -400\mu\text{A}$	2.4	—	V
$I_{CC1}$	Read Current	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}, \text{ all I/Os open, Address input} = V_{IL}/V_{IH}, \text{ at } f = 1/t_{RC} \text{ Min.}, V_{CC} = V_{CC} \text{ Max.}$	—	40	mA
$I_{CC2}$	Program Current	$\overline{CE} = \overline{WE} = V_{IL}, \overline{OE} = V_{IH}, V_{CC} = V_{CC} \text{ Max.}$	—	50	mA
$I_{SB}$	TTL Standby Current	$\overline{CE} = \overline{OE} = \overline{WE} = V_{IH}, V_{CC} = V_{CC} \text{ Max.}$	—	2	mA
$I_{SB1}$	CMOS Standby Current	$\overline{CE} = \overline{OE} = \overline{WE} = V_{CC} - 0.3\text{V}, V_{CC} = V_{CC} \text{ Max.}$	—	100	$\mu\text{A}$
$V_H$	Device ID Voltage for $A_9$	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	11.5	12.5	V
$I_H$	Device ID Current for $A_9$	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}, A_9 = V_H \text{ Max.}$	—	50	$\mu\text{A}$

**AC Electrical Characteristics**

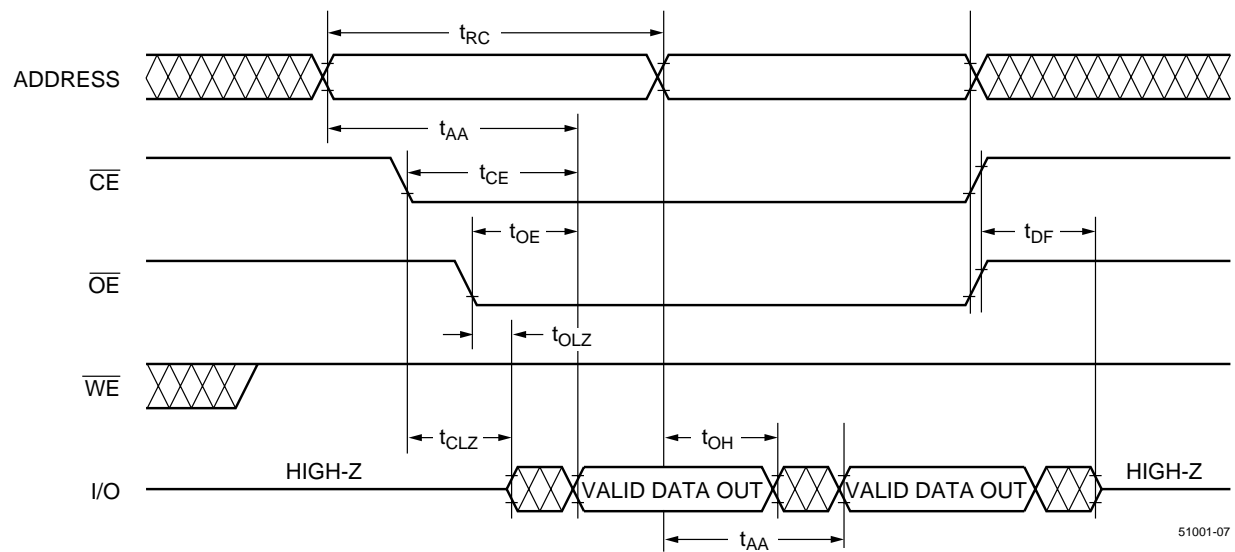
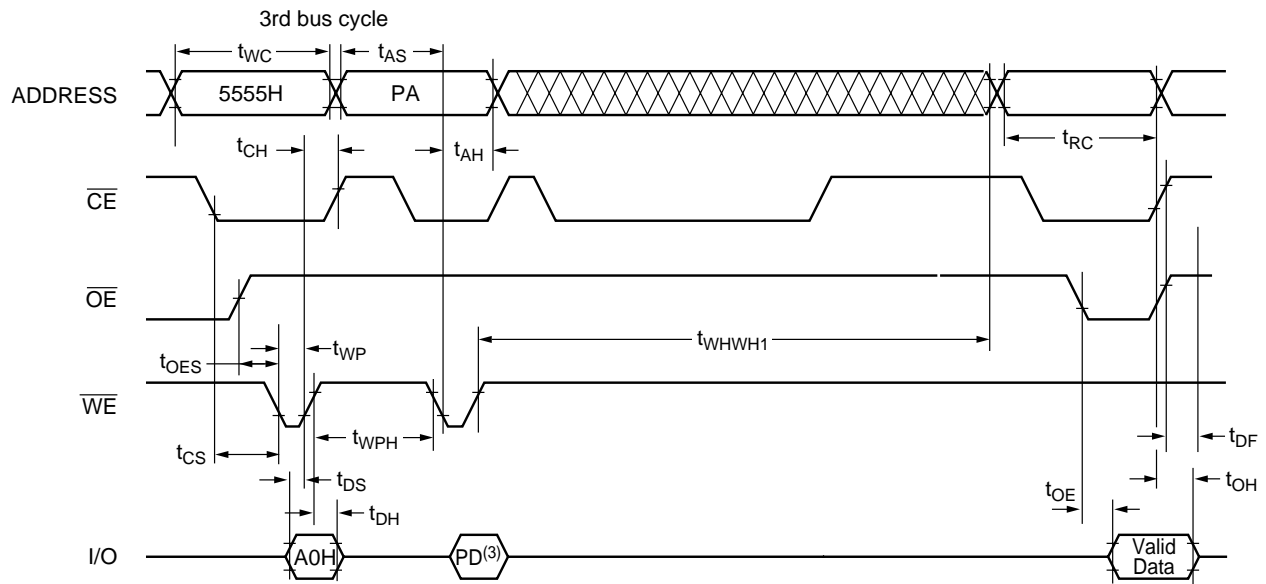
(over all temperature ranges)

**Read Cycle**

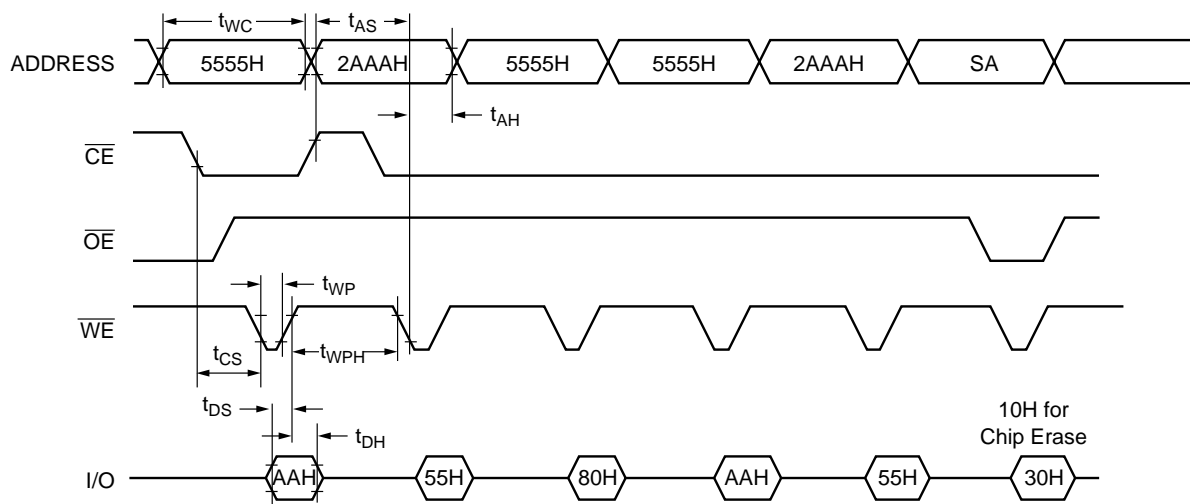
Parameter Name	Parameter	-90		Unit
		Min.	Max.	
$t_{RC}$	Read Cycle Time	90	—	ns
$t_{AA}$	Address Access Time	—	90	ns
$t_{ACS}$	Chip Enable Access Time	—	90	ns
$t_{OE}$	Output Enable Access Time	—	40	ns
$t_{CLZ}$	$\overline{CE}$ Low to Output Active	0	—	ns
$t_{OLZ}$	$\overline{OE}$ Low to Output Active	0	—	ns
$t_{DF}$	Output Enable or Chip Disable to Output in High Z	0	20	ns
$t_{OH}$	Output Hold from Address Change	0	—	ns

**Program (Erase/Program) Cycle**

Parameter Name	Parameter	-90			Unit
		Min.	Typ.	Max.	
$t_{WC}$	Program Cycle Time	90	—	—	ns
$t_{AS}$	Address Setup Time	0	—	—	ns
$t_{AH}$	Address Hold Time	45	—	—	ns
$t_{CS}$	$\overline{CE}$ Setup Time	0	—	—	ns
$t_{CH}$	$\overline{CE}$ Hold Time	0	—	—	ns
$t_{OES}$	$\overline{OE}$ Setup Time	0	—	—	ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	0	—	—	ns
$t_{WP}$	$\overline{WE}$ Pulse Width	45	—	—	ns
$t_{WPH}$	$\overline{WE}$ Pulse Width High	35	—	—	ns
$t_{DS}$	Data Setup Time	30	—	—	ns
$t_{DH}$	Data Hold Time	0	—	—	ns
$t_{WHWH1}$	Programming Cycle	—	—	30	$\mu$ s
$t_{WHWH2}$	Sector Erase Cycle	—	—	10	ms
$t_{WHWH3}$	Chip Erase Cycle	—	2	—	sec

**Waveforms of Read Cycle****Waveforms of  $\overline{WE}$  Controlled-Program Cycle****NOTES:**

1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.

**Waveforms of Erase Cycle<sup>(1)</sup>**

51001-10

**NOTES:**

1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.
3. SA: The sector address for Sector Erase. Address = don't care for Chip Erase.

**FUNCTIONAL DESCRIPTION****Read Cycle**

A read cycle is performed by holding both  $\overline{CE}$  and  $\overline{OE}$  signals LOW. Data Out becomes valid only when these conditions are met. During a read cycle  $\overline{WE}$  must be HIGH prior to  $\overline{CE}$  and  $\overline{OE}$  going LOW.  $\overline{WE}$  must remain HIGH during the read operation for the read to complete (see Table 1).

**Output Disable**

Returning  $\overline{OE}$  or  $\overline{CE}$  HIGH, whichever occurs first will terminate the read operation and place the I/O pins in the HIGH-Z state.

**Standby**

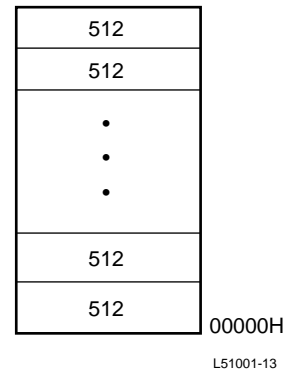
The device will enter standby mode when the  $\overline{CE}$  signal is HIGH. The I/O pins are placed in the HIGH-Z, independent of the  $\overline{OE}$  signal.

**Command Sequence**

The V29LC51001 does not provide the "reset" feature to return the chip to its normal state when an incomplete command sequence or an interruption has happened. In this case, normal operation (Read Mode) can be restored by issuing a "non-existent" command sequence, for example Address: 5555H, Data FFH.

**Byte Program Cycle**

The V29LC51001 is programmed on a byte-by-byte basis. The byte program operation is initiated by using a specific four-bus-cycle sequence: two unlock program cycles, a program setup command and program data program cycles (see Table 2).

**V29LC51001**

During the byte program cycle, addresses are latched on the falling edge of either  $\overline{CE}$  or  $\overline{WE}$ , whichever is last. Data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever is first. The byte program cycle can be  $\overline{CE}$  controlled or  $\overline{WE}$  controlled.

**Sector Erase Cycle**

The V29LC51001 features a sector erase operation which allows each sector to be erased and reprogrammed without affecting data stored in other sectors. Sector erase operation is initiated by using a specific six-bus-cycle sequence: Two unlock program cycles, a setup command, two additional unlock program cycles, and the sector erase command (see Table 2). A sector must be first erased before it can be reprogrammed. While in the internal erase mode, the device ignores any program attempt into the device. Sector erase is completed in 10ms max. The V29LC51001 is shipped with pre-erased sectors (all bits = 1).

**Table 1. Operation Modes Decoding**

Decoding Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$A_0$	$A_1$	$A_9$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$A_0$	$A_1$	$A_9$	READ
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	$A_0$	$A_1$	$A_9$	PD
Standby	$V_{IH}$	X	X	X	X	X	HIGH-Z
Output Disable	$V_{IL}$	$V_{IH}$	$V_{IH}$	X	X	X	HIGH-Z

**NOTES:**

1. X = Don't Care,  $V_{IH}$  = HIGH,  $V_{IL}$  = LOW.  $V_H$  = 12.5V Max.
2. PD: The data at the byte address to be programmed.



**Table 2. Command Codes**

Command Sequence	First Bus Program Cycle		Second Bus Program Cycle		Third Bus Program Cycle		Fourth Bus Program Cycle		Fifth Bus Program Cycle		Six Bus Program Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read	XXXXH	F0H										
Read	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	5555H	AAH	2AAAH	55H	5555H	90H	00H	40H(3)				
							01H	60H(4)				
Byte Program	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD(2)				
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	PA(1)	30H

**NOTES:**

1. PA: The address of the memory location to be programmed.
2. PD: The data at the byte address to be programmed.
3. 40H: Manufacturing ID
4. 60H: Device ID

**Chip Erase Cycle**

The V29LC51001 features a chip-erase operation. The chip erase operation is initiated by using a specific six-bus-cycle sequence: two unlock program cycles, a setup command, two additional unlock program cycles, and the chip erase command (see Table 2).

The chip erase operation is performed sequentially, one sector at a time. When the automated on chip erase algorithm is requested with the chip erase command sequence, the device automatically programs and verifies the entire memory array for an all zero pattern prior to erasure

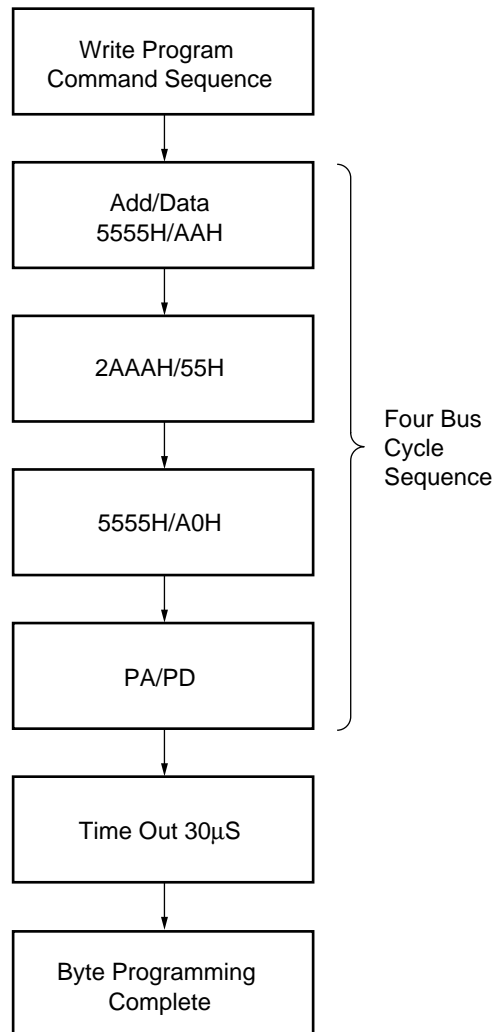
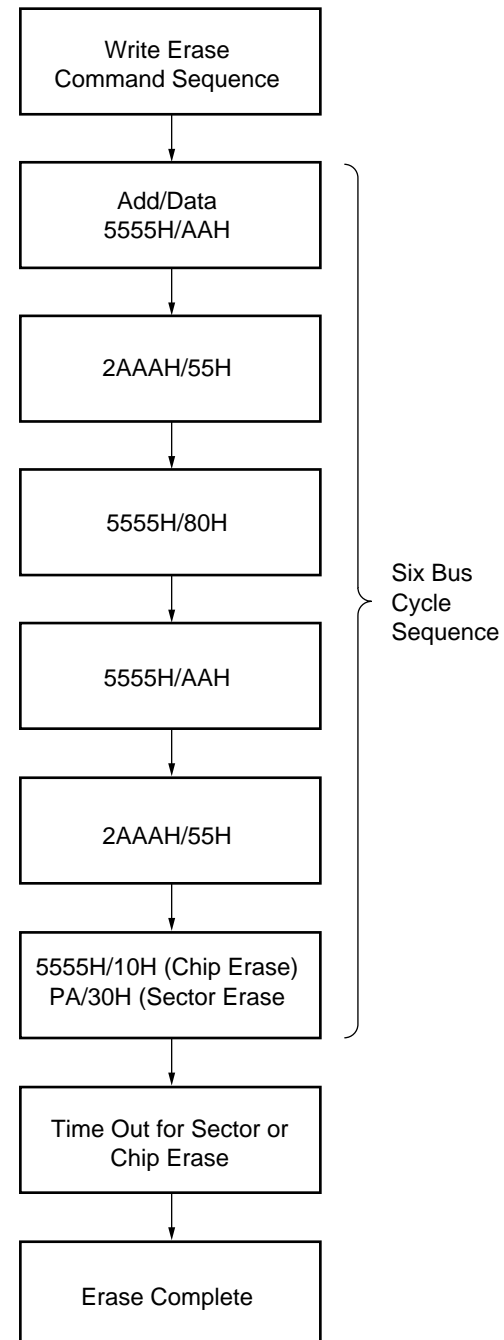
The automatic erase begins on the rising edge of the last  $\overline{WE}$  or  $\overline{CE}$  pulse in the command sequence and terminates 500ms later.

**Hardware Data Protection**

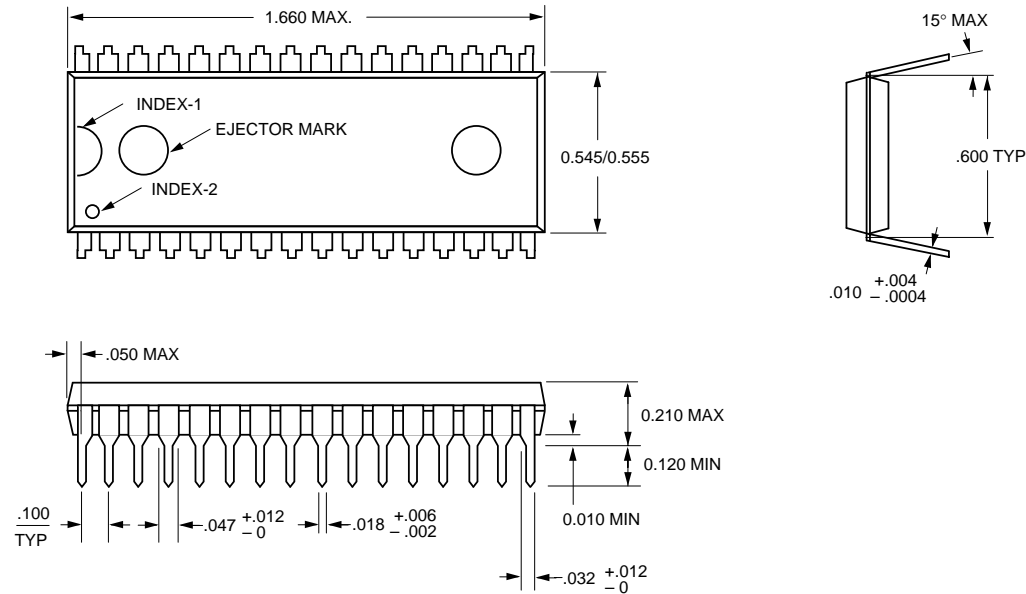
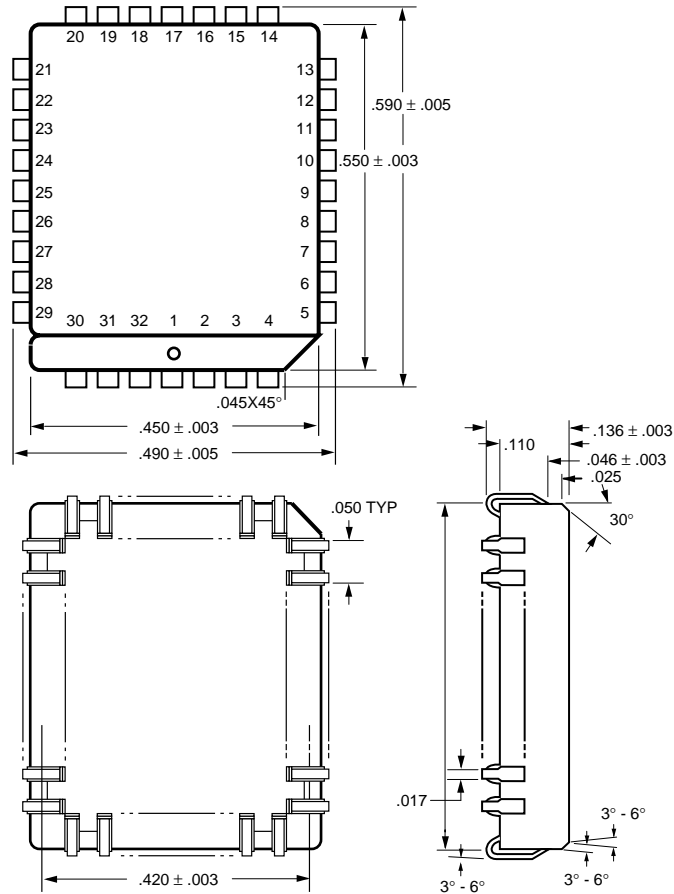
*V<sub>CC</sub> Sense Protection:* the program operation is inhibited when VCC is less than 2.5V.

*Noise Protection:* a CE or WE pulse of less than 5ns will not initiate a program cycle.

*Program Inhibit Protection:* holding any one of OE LOW, CE HIGH or WE HIGH inhibits a program cycle.

**Byte Program Algorithm****Chip/Sector Erase Algorithm**

L51001-14

**Package Diagrams****32-pin Plastic DIP****32-pin PLCC**

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